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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,129	10/14/2003	Koray Oner	BP 3255.3	4545

34399 7590 01/17/2006

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/685,129	**Applicant(s)** ONER ET AL.	
	Examiner Angel L. Casiano	**Art Unit** 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

The present Office action is in response to application dated 14 October 2003.

Claims 1-20 are pending. All claims have been examined.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

a. Figure 2: 200-205, 220, 258, and 260-265

b. Figure 3: 339, 343, 345, 346, 370, 375, and 380

c. Figure 6: 610-613 and 662-663

d. Figure 8: 81a, 81b, 82a, 82b, 83, 86, and 87

e. Figure 9: 93, 94, and 97

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because "[0122]" must be deleted. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

- Page 22, [074]; information must be updated
- Page 26, [085]; information must be updated

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2-4 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, this recites: "the apparatus recited in claim 1, comprising a data merge circuit coupled to store in a fragment storage register the sifted data..." (emphasis added). However, it is unclear to which element in the apparatus the data merge circuit is coupled to. Claim3 and 4 depend upon claim 2 and are therefore rejected under the same basis.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1. Determining the scope and contents of the prior art.
   2. Ascertaining the differences between the prior art and the claims at issue.
   3. Resolving the level of ordinary skill in the pertinent art.
   4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1 5, 7-11, 13-14, 16-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hocevar in view of.

Regarding claim 1, Hocevar teaches in an integrated circuit device (see Page 2, [0019]), an apparatus for transferring data from a first bus to a memory bus (see Figure 2, "20"), comprising: a first interface circuit (see Figure 2, "34") for receiving packet data and transferring the packet data to a first bus (see Figure 2, "B"); a memory bus (see Page 17, [0181] and [0178], *the circuitry is capable of handling a wide range of code widths*); a packet manager circuit (see Figure 2, "31") coupled between the first bus and the memory bus to transfer data received from the first interface circuit to memory, said packet manager circuit comprising, an input buffer (see Figure 8, "66A", "66B"; Page 11, [0123], *update circuit 60 is part of decoder 38, which is included in apparatus 31*) coupled to the first bus; an alignment circuit (see Figure 8, "63" and "75") coupled to the input buffer for shifting data (see Page 11, [0123], *aligners 63, 75 are effectively shifters that can be used to align the incoming and outgoing data words as desired or necessary*) stored in the input buffer to output shifted data; and a controller (see Page 11, [0123]; *address generator circuit 68 controls the addressing of column sum memories 66A, 66B*) for controlling the shifting of data in the alignment circuit and for writing the shifted data to the memory bus.

However, the Hocevar reference does not teach a first descriptor for controlling the transfer of data by a packet manager circuit. As for this limitation, Lang et al. teaches a descriptor for controlling the transfer of packet data (see col. 2, lines 21-31). Accordingly, at the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain an apparatus for encoding and decoding data communicated over multiple data links, according to a data link control protocol, such as high level data link control (HDLC), as taught by Lang et al (see col. 1, lines 4-7).

As for claim 5, Hocevar does not disclose the buffer circuits (see "66A", "66B") as comprising FIFO buffers. As for this limitation, Lang et al. teaches a packet management circuit where incoming data segments are stored in receive side channel first-in-first-out (FIFO) buffer of packet buffer processor (see col. 30, lines 21-44). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above, in the rejection of claim 1.

As for claim 7, Hocevar fails to teach data transfer on a plurality of channels from a first bus to a memory bus, wherein an input buffer comprises a buffer region for each of the plurality of channels, as claimed. As for this limitation, Lang et al. teaches a plurality of channels having each a region in a FIFO buffer (see col. 4, lines 14-16). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above, in the rejection of claim 1.

As for claim 8, Hocevar fails to teach the use of register files for storing intermediate values for packets and states for the plurality of channels. Lang et al. teaches the use of register for storing intermediate values for packets (see col. 31, lines 5-7; *each time said holding register is updated with data by said serial-to-parallel converter*) and states for the plurality of channels (see col. 31, lines 8-13; *clock activity monitor comprises a threshold register*). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above, in the rejection of claim 1.

Regarding claim 9, the combination of Hocevar in view of Lang et al. teaches an apparatus for transferring data from a first bus to a memory bus (see rejection of claim 1). This apparatus includes a packet manager circuit (see *supra*). Therefore, the combination of references also teaches the packet manager circuit having an apparatus for aligning and merging packet fragments. The present claim is rejected under the same rationale.

As for claims 10-11 and 13-14 the combination of Hocevar in view of Lang et al. teaches an apparatus for transferring data from a first bus to a memory bus (see rejection of claim 1). This apparatus includes a packet manager circuit (see *supra*). Therefore, the present claims are rejected under the same rationale.

Regarding claim 16, the combination of Hocevar in view of Lang et al. teaches an apparatus for transferring data from a first bus to a memory bus (see rejection of claim 1). Therefore, the combination of references also teaches the method directed to the apparatus. The present claim is rejected under the same rationale.

As for claims 17-18 and 20, the combination of Hocevar in view of Lang et al. teaches an apparatus for transferring data from a first bus to a memory bus (see rejection of claim 1). Therefore, the combination of references also teaches the corresponding method. The present claims are rejected under the same rationale.

Allowable Subject Matter

11. Claims 2-4, 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 recites, inter alia; a data merge circuit coupled to store in a fragment storage register the shifted data from the alignment circuit (as in claim 1) that is not written to memory in a first data cycle. The data merge circuit combines data stored in the fragment storage register with data stored in the input buffer in a second data cycle to form a merged data value that is written to the memory bus. The references of record do not teach or suggest the aforementioned limitations, nor would it be obvious to modify these references to include such limitation. Claim 12 contains similar allowable limitations, directed to the packet manager circuit.

Claims 3 and 4 depend upon claim 2 and therefore also include allowable subject matter.

13. Claims 6, 15 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 recites, inter alia; an alignment circuit (as in claim 1), comprising a fragment storage buffer for storing a portion of a first packet fragment that has been stored in an input buffer and shifted to created a first data alignment. The claim also discloses that this first data fragment is merged with a portion of a second packet fragment that has been stored in the input buffer and shifted to create a second data fragment. The references of record do not teach or suggest the aforementioned limitations, nor would it be obvious to modify these references to include such limitation.

Claim 15 contains similar allowable limitations, directed to a packet manager circuit.

Claims 19 contain similar allowable limitations, directed to the method for aligning and merging packet data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
05 January 200~~5~~ 6

KIM HUYNH
SUPERVISORY PATENT EXAMINER
1/8/06